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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,385	STEISS ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7,8,10-16,22,23,25-33,35,37,38 and 40-47* is/are rejected.

7)☒ Claim(s) *2-6,9,17-21,24,34,36,and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,7,8,10-13,14,15,16,22,23,25-28,29,30,31,37-38,40-43,44,45,46,47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eikemeyer (patent No. 6,931,639) in view of Kalla (patent No. 7,013,400 and Kottapalli (patent application publication 2002/0087840).

3. Eikemeyer taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Fetch control unit ((206,208) having an input coupled to receive an execution feedback signal (output from completion control unit 224) with the fetch control unit generating an instruction fetch sequence based on the execution feedback signal (e.g., see col. 3, lines 15-37); and

b) An instruction cache (202), having an input coupled to an output of the fetch control unit (e.g., see fig. 2), the instruction cache dispatching instruction data responsive to the instruction fetch sequence (e.g., see col. 3, lines 15-37).

Eickmeyer did not expressly detail (claims 1,14,16,29, 31,40,44,46) that the information was information related to a plurality of threads on a per thread basis. Kalla however taught (e.g., see col. 6, lines 45-59) the information from the completion unit

comprises information from completion tables indicating which instructions from plural threads from the various execution units were completed, Therefore one of ordinary skill would have motivated to store the status information from different threads in separate ones of the completion tables where the output of the completion tables that was fed to the fetch unit would have been on a per thread basis. Also since the data from the various execution units would have been used again by a particular execution unit in execution a particular type of thread then one of ordinary skill would have been motivated to keep track of which thread the data was generated at least so that the data would be sent to the appropriate area of the cache that would have stored data for a particular execution unit. Eickenmeyer and Kalla did not specifically detail that the feedback signal had stall information relating to a thread plurality of thread on a per thread basis. Kottapalli However taught this limitation (e.g., see figs. 1, 2, and paragraphs 0010-0013)[on a stall the exception and retirement logic 107 informs fetch unit to fetch the miss instruction from thread "0". This would have required a feedback signal and a feedback signal is shown between exception and retirement logic 107 and fetch unit 101 in fig. 1]. As per claim 7,8,22,23,37,38 this scheduler 104 along with exception and retirement unit performed operations for interleaving the thread and indication that a thread was stalled and ineligible for execution and flushed(e.g., see paragraphs 0010-0013) and along with the feedback as discussed above.

Further as to claims 10,25 Kottapalli taught the pipeline output at the exception and retirement unit is fed back to the fetch unit for fetching instructions (e.g., see fig. 1).

As per claims 11,12,26,27,41,42 Kottapalli taught delaying the thread responsive to the execution stall and the stall due to a exception or cache miss(e.g., see paragraph 0013).

One of ordinary skill would have been motivated to combine the teachings of Eickemeyer and Kottapalli. Both references were directed to the problems of providing efficient processing of threads in a DP system. One of ordinary skill would have been motivated to incorporate the Kottapalli teachings of feedback for stalled thread at least to provide an efficient way to recovery from a stalled thread.

4. As per claims 13,28,43 Kalla taught wherein the fetch control unit generates the instruction fetch sequence, in a default state, by selecting a thread from the plurality of threads according to an alternating selection using two threads providing equal amount of fetching between threads , but did not specifically detail a round robin scheme. However since when using more than two threads the plural fetch equally between threads would occurred for plural threads in a round robin manner and the use of round robin arbitration was well known in the art at the time of the claimed invention one of ordinary skill would have been motivated to use round robin arbitration between threads for fetching to ensure that the each thread was had enough instructions fetched (e.g., see fig. 1 and col. 6, lines 4-18).

5. As per claims 15,30,45 Eikemeyer and Kalla taught a multithreaded processor as discussed above. The application of a multi-threaded processor for processing multiple network thread would have provided a parallel processing of threads and therefore more efficient processing of the threads. Consequently one of ordinary skill in the DP art

would have been motivated to apply the Eikemeyer and Kalla system to processing network data and therefore provide a network processor which characteristically would process packets in a routing switching bridging and forwarding operations which were conventional operations performed in networked processors.

6. It would have been obvious to one of ordinary skill in the DP art at the time of the claimed invention to combine the teachings of Eikemeyer and Kalla. Both references were directed to the problems of processing instruction threads in a DP system. One of ordinary skill would have been motivated to incorporate the Kalla teachings of coupling feedback from the output of the execution units via a completion unit to the fetch unit and provide status signals from the threads via the completion unit at least to ensure that each thread ready for instructions or data had the instructions fetched from the cache in a prompt manner.

7. As per claim 47, Eickemeyer , Kalla and Kottapolli taught system that providing for multithreading where some thread would have been active and some not active where at least two active thread would have been processed and therefore it would have been within the skill of one of ordinary skill in the DP art to implement the combined system with more than two threads(e.g., see col. 2, lines 4-67 of Kalla).

Claims 32-33, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eickemeyer and Kalla and Kottapalli as applied to claims 1,31 above, and further in view of Boggs (patent No. 7,051, 329).

8. As per claim 32, Boggs taught an instruction queue (238)(e.g., see col. 17, line 4-col. 18,line 1) having an output coupled to the fetch control unit input, the instruction

queue generating a queue feed back signal responsive to a thread queue condition associated with a thread from the plurality of threads (e.g., see figs. 16, 17 and col. 1, line 1-col. 19, line 23).

9. As per claims 33, Boggs taught wherein the thread queue condition indicates that a thread queue has less than a first amount of remaining storage (e.g., see col. 21, line 11-col. 22, lines 23).

10. As per claim 35, Eikemeyer taught storing entries for plural threads in a single queue (e.g. see fig. 4). Therefore one of ordinary skill would have been motivated to maintain the amount of instructions for each of the plural instructions and therefore indicate that a thread queue has less than a second amount of remaining decoded instructions [a second amount for a second thread in the same queue].

It would have been obvious to one of ordinary skill in the DP art at the time of the claimed invention to combine the teachings of Eikemeyer and Boggs. Both references were directed to the problems of processing instruction threads in a DP system. One of ordinary skill would have been motivated to incorporate the Boggs teachings of queue fetch control signals used to control the processing of threads at least to provide sufficient instructions and data to each for each of the threads.

Allowable Subject Matter

11. Claims 2-6,9,17-21,24,34,36,39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-47 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bondi (patent No. 5,881,277) disclosed a pipelined multiprocessor with feedback from execution stage to fetch stage(e.g., see abstract and fig. 2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ERIC COLEMAN
PRIMARY EXAMINER